APPLICATION NOTE

ProTek Devices' ESD Protection in USB3.0 Applications

Version 3.0 of the Universal Serial Bus (USB) specification offered a generational leap in performance capabilities over USB 2.0. It increases the data rates by 10 times. It also expands transmission lines to 3 differential pairs (compared to 1 in the previous 2.0 generation). USB was introduced in 1996 with version 1.0. It provided 1.5Mbit/sec in Low-Speed (LS) mode and 12Mbit/sec in Full-Speed (FS) mode. In the year 2000 USB 2.0 entered the market. The new High-Speed (HS) mode serves up to 480Mbit/sec. It was still downwards compatible to Low-Speed and Full-Speed mode. At present, USB2.0 is one of the most widespread, general-purpose external data interfaces. It has become the default standard interface in all computer systems.

The USB2.0 interface is also widely used in consumer electronics. Devices such as, camcorders, digital cameras, digital music players, game consoles, DVD/Blue-Ray players and TVs use USB. It's also widespread in portable devices such as, smartphones and in networking equipment like DSL/router units.

In November 2008 the USB3.0 specification was released and demonstrated full USB2.0 functionality (HS, FS, LS). It also showcased the new separate ultra high speed data link, called SuperSpeed™. The SuperSpeed link works with separate differential data lines for download (Host => Device, called TX direction). This is also the case for upload in RX direction (Device => Host). The maximum data rate in SuperSpeed mode is 5Gbit/sec. The combination of USB2.0 functionality and the new SuperSpeed mode requires new cable construction. The construction must serve 3 differential coupled signal lines (TX+/Tx-, RX+/Rx- and D+/D-). The VCC and the GND line complete the cable set.

Design Considerations

The following design considerations for the entire USB3.0 link should be observed:

- Full impedance-matched 90 Ohm differential design for all PCB lines and interconnection cables are mandatory.
- Non-differential coupled lines have to be minimized. They have significant impact to eye pattern inner eye opening.
- Trace-width and trace-separation of the 90 Ohm differential: coupled PCB traces should not be too narrow to avoid additional loss and being robust enough for manufacturing. A trace-width of 0.007"(0.178mm) and a separation of 0.007"(0.178mm) between the differential traces would be ideal for production.
- Identical delay (trace length) between the positive and the negative line (including the USB3.0 cable) of the differential coupled link (minimizing in pair skew) is needed. This is important to keep signal integrity high and to avoid common mode reflection.

A layout example for the USB3.0 standard-A connector section in combination with ESD protection devices is shown in Figure 1.

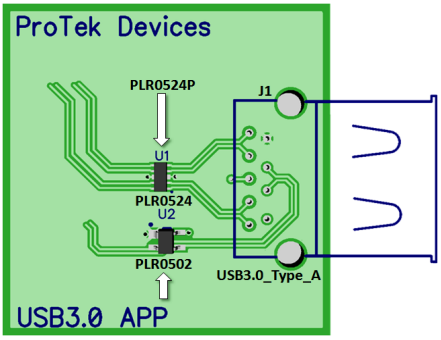

Figure1: Layout recommendation.

In Figure 1, the SuperSpeed TX and RX data pairs are protected by ProTek Devices' PLR0524P. The D+ D- regular USB2.0 pair is protected by ProTek Devices' PLR0502. The PLR0502 has an internal transient voltage suppressor (TVS) that also protects the VCCBUS. The PLR0524P has an ultra low line to ground capacitance of 0.8pF. This is ideal for use in the high speed application. The PLR0502 has a line to ground capacitance of 0.6pF. Fig.2. shows an exploded view of a standard USB3.0 connector.

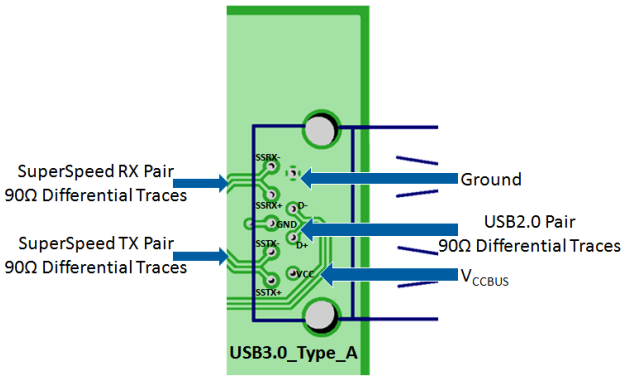

Figure 2: Exploded view of the USB3.0 standard connector.

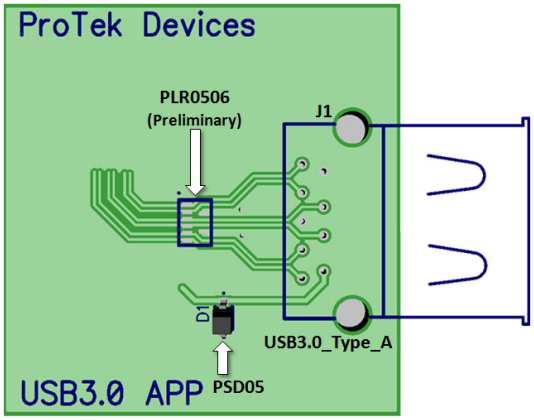

Figure 3: Suggested layout of the PLR0506.

An alternate layout is possible, as shown in Fig.3. Here, all SuperSpeed and regular speed (USB2.0) data lines are protected by one device, ProTek Devices' new PLR0506 (Preliminary). The PLR0506 is configured in a miniature 3.3 x 1.3 mm DFN-8 package. This provides significant space-saving real estate on PCBs. The line to ground capacitance is 0.8pF. Protection for the VCCBUS is provided by ProTek Devices' PSD05.

Figure 4 is an exploded view showing the flow through trace design.

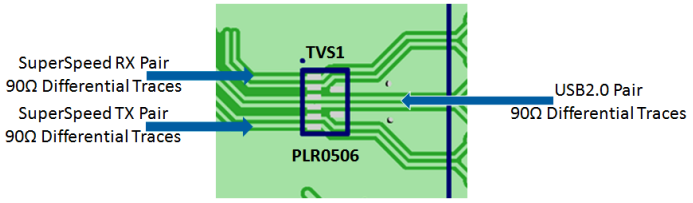

Figure 4: Exploded view of PLR0506 showing flow through design.

Small Footprint Needs

Miniaturization of ESD protection devices has introduced additional problems. This includes higher clamping and less robustness compared to larger die geometries. ProTek Devices' new chip designs have alleviated this problem. The PLR0524P clamping for a 8kV contact discharge, per IEC 61000-4-2, is a very low ~6 V measured at the 30nSec point. It is demonstrated in Figure 5.

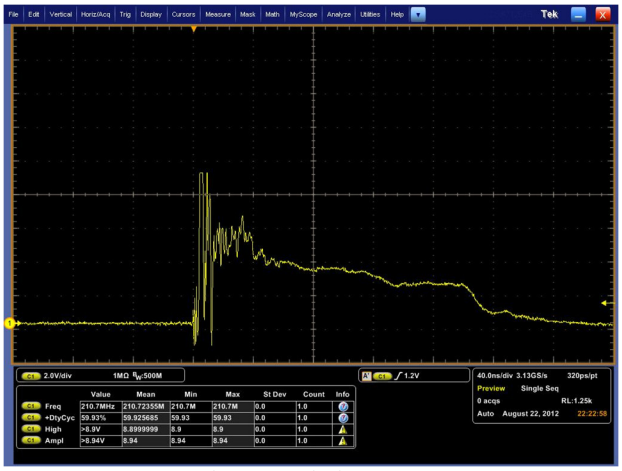

Figure 5: +8kV contact discharge IEC 61000-4-2.

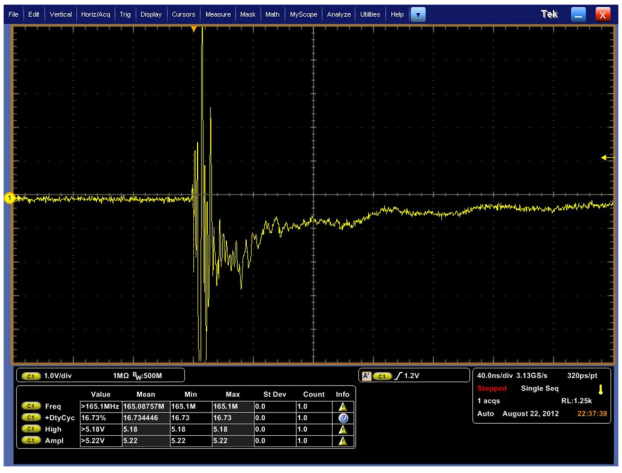

Figure 6: -8kV contact discharge IEC 61000-4-2.

For the PLR0524P -8kV ESD discharge the clamping is typically around one diode drop (1.2V) to ground. The steering diode will conduct directly to ground and this is shown in Figure 6.

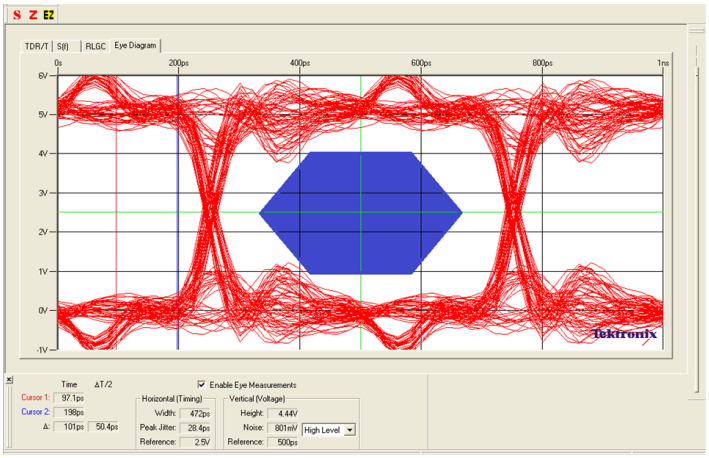

Figure 7: Eye diagram of the USB3.0 application with PLR0524P in circuit.

The eye diagram of the PLR0524P shows that the line capacitance has very little effect on the eye mask. Ultra high speed data transmission systems have a severe design obstacle. Designs must ensure a certain level of signal integrity at a receiver. High signal integrity is important to achieve a low bit error rate (e.g. for USB3.0 SuperSpeed a bit error rate of 1E-12 is typical). The signal integrity is characterized by the eye diagram.

In a perfect system without limitation in bandwidth, the eye diagram would be perfectly open. In a real system, the signal rise-time/fall-time is limited by the TX and the RX impedance (90 Ohm differential). And, this is in combination with all parasitic capacitance at TX side and RX side. These parasitic capacitances are inside the USB3.0 transceiver, and/or externally on the PCB. External parasitics can be caused by unmatched PCB lines, the USB3.0 connector, or other shunt capacitors. Values of shunt capacitors are to be kept as small as possible. The low pass frequency response of the USB3.0 cable has to be taken in to account as well. To compensate the attenuation of high frequency content, the signal is tuned by a dedicated equalization on TX and on RX side.

Both measures help speed up the signal at the rising and falling edges which results in a more open eye diagram (better signal integrity; Figure 7).

Conclusion

USB3.0 and SuperSpeed have ushered in many new cable construction design requirements. One design consideration includes ESD protection. However, the continued miniaturization of ESD protection devices has introduced its own problems. They include higher clamping and less robustness compared to larger die geometries. ProTek Devices' new chip designs alleviate all such problems. The new chip designs are well suited to provide ESD protection in USB3.0 applications.